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A DIGITAL VOLTAGE-CONTROLLED OSCILLATOR FOR PHASE LOCK LOOPS

by Dominick E. Santarpia and Thomas E. McGunigal

Goddard Space Flight Center
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ABSTRACT

This report describes the development of a Digital Voltage-Controlled Oscillator Phase Lock Loop. A large frequency-tracking range and high phase stability are conflicting requirements of a conventional voltage-controlled oscillator (VCO); however, a digitally controlled frequency synthesizer performing in place of the conventional tracking oscillator will provide the stability and spectral purity of a very good 1-MHz standard over very wide frequency excursions.

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INTRODUCTION

A key component in the design of tracking and telemetry receivers is the carrier-loop voltage-controlled oscillator (VCO). The VCO must provide sufficient frequency-pulling range to accommodate doppler shifts; however, a large pulling range is difficult to achieve since the VCO must be sufficiently stable to operate in a narrow tracking loop without contributing significant loop phase error.

A large pulling range and high phase stability are conflicting requirements of a VCO (Reference 1). For example, a wide pulling range requires a low resonator Q, while good stability requires a high resonator Q. It seems, at first, that what is wanted is a compromise design; and this may not fully satisfy either requirement.

However, the unique characteristics of coherent frequency synthesizers now make possible the generation of RF signals over a wide frequency range without sacrifice of stability or accuracy and, hence, the digital voltage-controlled oscillator discussed herein. This has been designed as a carrier loop VCO that does not demand the aforesaid compromises.

GENERAL DESCRIPTION

Figure 1 is a block diagram of a digital VCO and the associated phase lock loop. The phase detector, loop filter, loop dc amplifier, and 1 MHz VCO constitute a conventional second-order phase lock loop (References 2 and 3). The frequency synthesizer is driven by the 1 MHz VCO and coherently synthesizes frequencies up to 50 MHz; thus, it is essentially a frequency multiplier. As the input frequency varies (because of doppler shift, for example) loop phase error builds up in order to shift the VCO frequency. The digital controller is designed to read the loop error voltage and step the wide-range synthesizer in frequency when a voltage level determined by the VCO pulling range has been reached, thereby reducing the phase error to zero. The 1 MHz VCO can thus have a narrow frequency-pulling range and good stability while operating in a narrow loop with a large tracking range.

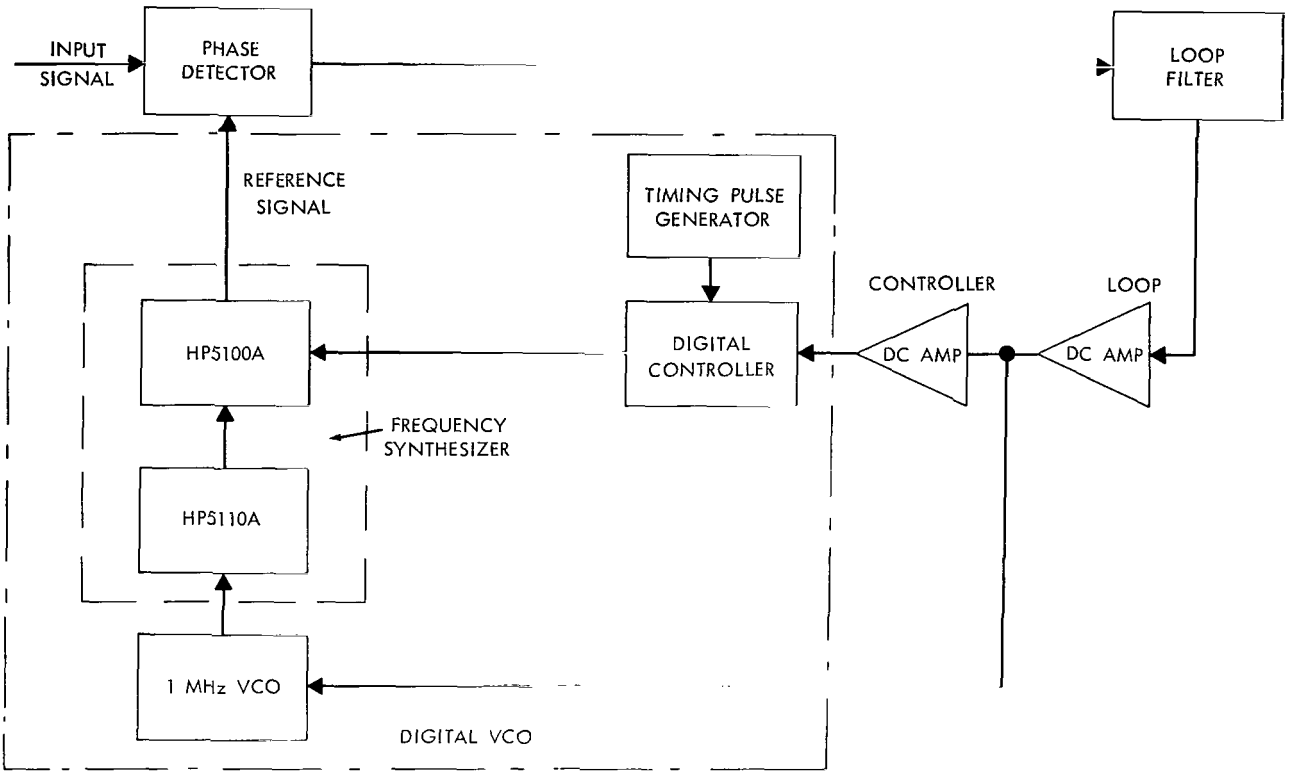

Figure 1—Block diagram of digital VCO phase lock loop.

The phase lock loop employed is a narrow-band second-order loop designed to track large doppler-frequency excursions. The phase detector compares the phase of the input signal with the phase of the reference signal. The output voltage of the phase detector is a measure of the phase difference between its two inputs. This error voltage is filtered by a low-pass filter which suppresses noise and high-frequency signal components. The filter also helps to establish the dynamic performance of the loop. The filtered error voltage is then amplified by the loop dc amplifier and applied to the VCO, thereby changing the frequency in a direction that reduces the phase difference between the input and reference signals. The controller dc amplifier provides the additional gain and the impedance level necessary for operation of the controller. The controller has an additional input, a pulse-train signal whose pulse repetition frequency is adjustable. The purpose of this second input will be made clear later.

FREQUENCY SYNTHESIZER/CONTROLLER

The frequency synthesizer is a frequency multiplier whose multiplication factor can be varied in small steps. This is accomplished by applying on or off voltages to a diode switching matrix in the synthesizer. For the control of four decades as described here, 40 separate lines are required. The role of the controller is to switch the proper voltages to the 40 separate lines that control the

aforesaid four decades. This switching must be done according to the two controller inputs, i.e., the loop phase error and the timing pulse. The controller consists entirely of logic circuits that primarily implement logical "and/or" expressions. The input circuits of the controller are voltage comparators that are biased to provide an "up" or "down" frequency count when the conditions previously discussed are all present. The output circuits are drivers designed to provide the proper voltage switching levels and impedance to the HP 5100A synthesizer.

Since the experimental controller was designed to control only four decades of the HP 5100A synthesizer, it is limited to switching over a 100 kHz range in 10 Hz increments. The controller could be expanded to count over a greater number of decades using identical circuit logic.

The pulse repetition frequency of the timing pulse generator must be adjusted according to the loop response time. This is because the synthesizer can switch much faster than the loop can respond. Thus, if the controller were not inhibited by the timing pulses, the synthesizer would switch many times before the loop could respond to the first change.

DESIGN CONSIDERATIONS

The loop selected for use in conjunction with the digital controller is conventional. Tests showed that the actual loop parameters closely agreed with the design values. The loop had an equivalent noise bandwidth of 27.7 Hz and could track doppler rates up to 100 Hz/sec. The natural frequency and 3-db frequency were 35 rad/sec and 17.5 Hz, respectively. The loop had a damping factor of 1.5 and a hold-in range of approximately 1 kHz. Results of tests to determine pull-out frequency (i.e., the frequency-step limit below which the loop does not skip cycles but remains locked) agreed with theoretical data published by Viterbi (Reference 4). According to his relationship between pull-out frequency, natural frequency, and damping factor, the pull-out frequency is on the order of 25 Hz. Therefore, synthesizer switching was accomplished in frequency increments less than this value in order to ensure that the digital VCO phase lock loop did not skip cycles during operation. For convenience the controller was adjusted to step the synthesizer in 10 Hz increments, although the HP 5100A can be stepped in increments as low as 0.01 Hz. The gain characteristics of the 1 MHz VCO determine the smallest increment by which the synthesizer can be stepped. For the particular loop designed, a 0.01 Hz change in the loop frequency of 50 MHz corresponds to an error voltage to the 1 MHz VCO of about 10^{-4} volt. In order to keep the error-voltage switching threshold at a practical level, 10 Hz switching increments were selected.

LOOP OPERATION, TEST RESULTS, AND MODIFICATIONS

For the test about to be discussed the digital VCO loop (B_L = 27.7 Hz) was locked to an input signal of approximately 50 MHz swept in frequency. As the input signal changes in frequency, the loop error voltage changes so as to pull the 1 MHz VCO over a range of 0.2 Hz, which corresponds to a 10 Hz change at the synthesizer output. At this point the error voltage to the controller reaches the preset threshold level. The controller then switches the synthesizer frequency by 10 Hz.

Since the error voltage to the 1 MHz VCO cannot go to zero at the instant of switching, the loop experiences a step change in frequency. If the change is less than the pull-out frequency of the loop, the loop remains locked. The loop recovers from the step change to track the incoming signal until another step change occurs; then the process repeats itself.

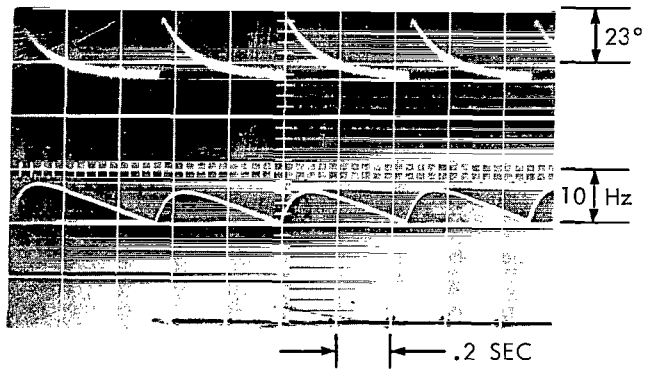

Figure 2—Oscillogram of phase detector output for "up" frequency step changes (top trace), error voltage to controller (bottom trace). Loop BW = 27.7 Hz.

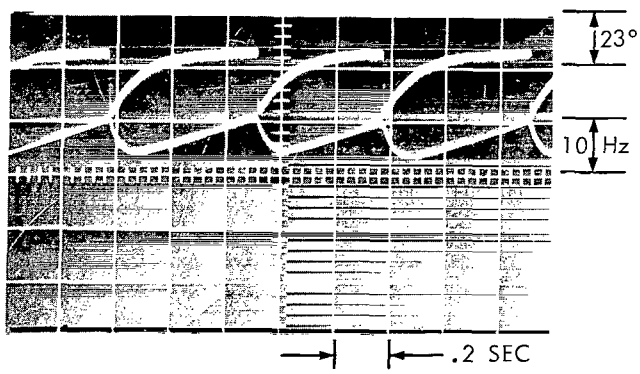

Figure 3—Oscillogram of phase detector output for "down" frequency step changes (top trace), error voltage to controller (bottom trace). Loop BW = 27.7 Hz.

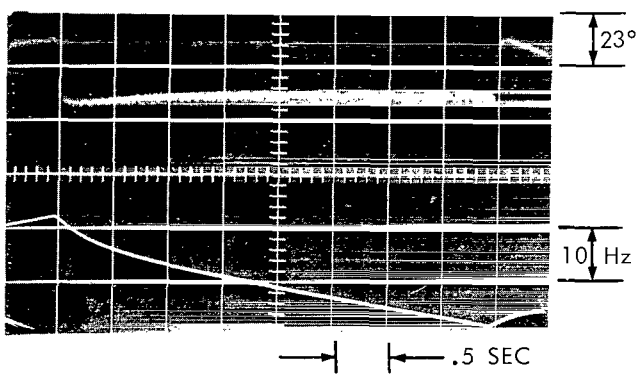

Figure 4—Oscillogram phase of detector output showing transition from "down" to "up" frequency switching (top trace) and error voltage input to controller (bottom trace). Loop BW = 27.7 Hz.

The top trace of Figure 2 shows the loop phase detector output for an increasing frequency change of the loop input signal. The second trace describes the error voltage input to the controller, translated in terms of the frequency change of the loop input signal. Note the transient phase error at the instant of switching. The phase detector output waveform corresponds to an approximate 23-degree peak-to-peak phase error.

Figure 3 shows the output of the phase detector and the input to the controller for decreasing changes in the input signal frequency. Figures 4 and 5 show these outputs for the transition between increasing and decreasing frequency changes in the loop input signal.

In order to demonstrate the effect of loop bandwidth on phase error, a wider loop of approximately 277 Hz was constructed, and the output of the phase detector observed. Figure 6 is an oscillogram of the phase detector output representing approximately 3.75 degrees p-p of phase error for a 10 Hz step change in frequency.

To demonstrate that the loop remained locked at all times, the output of the digital VCO was fed to a frequency discriminator. The output of the discriminator was observed during 10 Hz step changes in frequency; Figure 7 is an oscillogram taken at that time. The discriminator output shows that the loop did not skip cycles during this period. However, there was a time during the sweep when the loop did lose lock, as can be seen from Figure 8. Loss of lock (break in curve) occurred for each step change to a new decade, e.g., from 90 Hz to 100 Hz or from 990 Hz to 1 kHz.

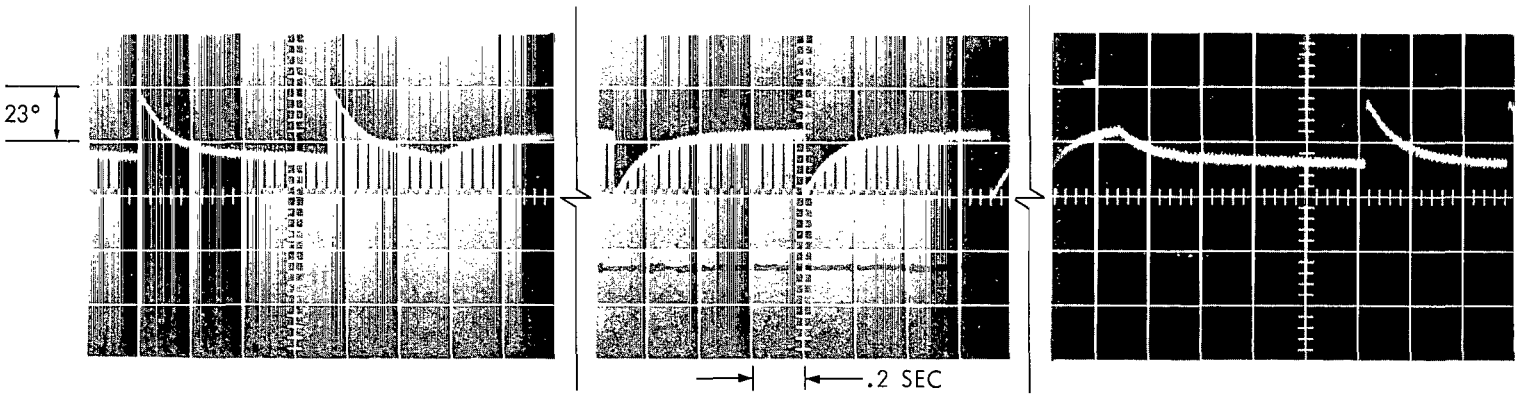

Figure 5—Oscillogram of phase detector output for "up" and "down" frequency step changes. Loop BW = 27.7 Hz.

A limitation on the generation of an accurate frequency output is introduced by the propagation delay of a signal through a decade in the HP 5100A synthesizer (Reference 5). Bandwidth-limiting circuitry in the 5100A decades causes a frequency change in one decade to be delayed at the output of the following decade by 4 microseconds relative to a change in that decade. These decade delays will cause a frequency error at the output of the synthesizer for a period of 4 μsec/decade; e.g., a change in frequency that effects a change of four decades will produce a declining frequency error that lasts for approximately 16 microseconds. Suppose that the controller has switched the synthesizer from 49,995,000 Hz to 49,995,090 Hz in 10 Hz steps. The controller now attempts to switch the synthesizer to 49,995,100 Hz; however, the frequency output of the synthesizer first changes to 49,995,190 Hz approximately 2 microseconds after the switching signal and then changes to 49,995,100 Hz 4 microseconds later. The frequency error of 90 Hz (for 4 microseconds) is large enough for the loop to lose lock for a short period of time. Likewise an incremental change in synthesizer frequency from 49,995,990 Hz to 49,996,000 Hz results in a declining frequency error of 990 Hz for 4 μsec and 90 Hz for an additional 4 microseconds.

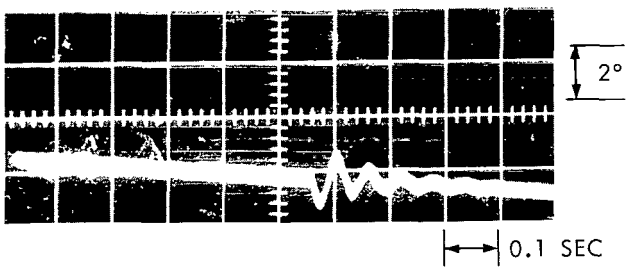

Figure 6—Oscillogram of phase detector output for "down" frequency step changes. Loop BW = 277 Hz.

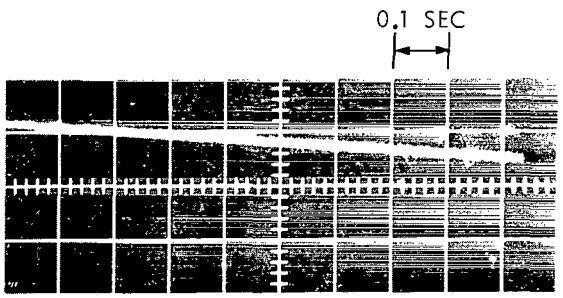

Figure 7—Oscillogram of discriminator output for frequency steps less than "pullout" frequency of loop.

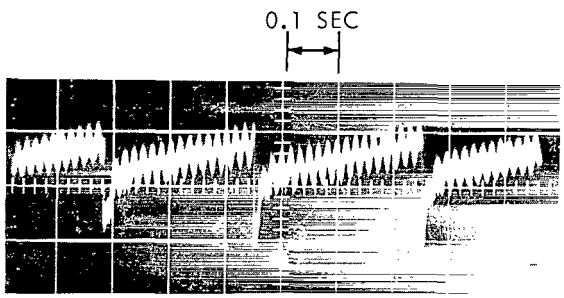

Figure 8—Oscillogram of discriminator output for frequency steps greater than "pullout" frequency of loop.

Because of this limitation, modification of the digital VCO loop was required so that a high-lock confidence level could be established. Figure 9 shows a block diagram of the modification to the digital VCO loop. A clean-up loop was designed to track the synthesizer output frequency and thereby the input signal to the loop, without tracking the short-duration frequency error produced by decade delays in the synthesizer. The clean-up loop operating on a high signal-to-noise output from the HP 5100A increases the pullout frequency of the digital VCO loop while not affecting the dynamics of the primary loop. It is important that the clean-up loop have a response time greater than the total synthesizer decade delay time and the clean-up loop bandwidth be much greater than the primary loop bandwidth.

Since the equipment originally used for the discriminator circuit was now used for the clean-up loop, other means for a loop lock check were derived. Figure 10 shows the lock-check circuit implemented.

The modulated input signal whose carrier frequency was approximately 50 MHz was fed to the primary phase detector of the digital VCO loop (B_L = 277 Hz) and to an HP 5245L counter for frequency division. The 5 MHz output of the counter was then frequency-divided by 5 by an HP 5110A Synthesizer Driver. The 1 MHz signal obtained was used as the reference signal or time base for an HP 5245L counter. The clean-up-loop VCO output was fed to the primary phase detector and the HP 5245L counter for a frequency check. Since the counter time-base frequency is always 50 times smaller than the clean-up-loop VCO frequency, the counter readout will always be 50 MHz (± an ambiguity of 1 count) if the clean-up loop VCO remains locked to the input signal and does not track the decade frequency error of the synthesizer.

At all times during operation of the modified digital VCO loop, there was no indication from the lock check circuit of the clean-up-VCO losing lock with the input signal. The lock check circuit also provided the means to determine the peak-to-peak phase error from the primary phase

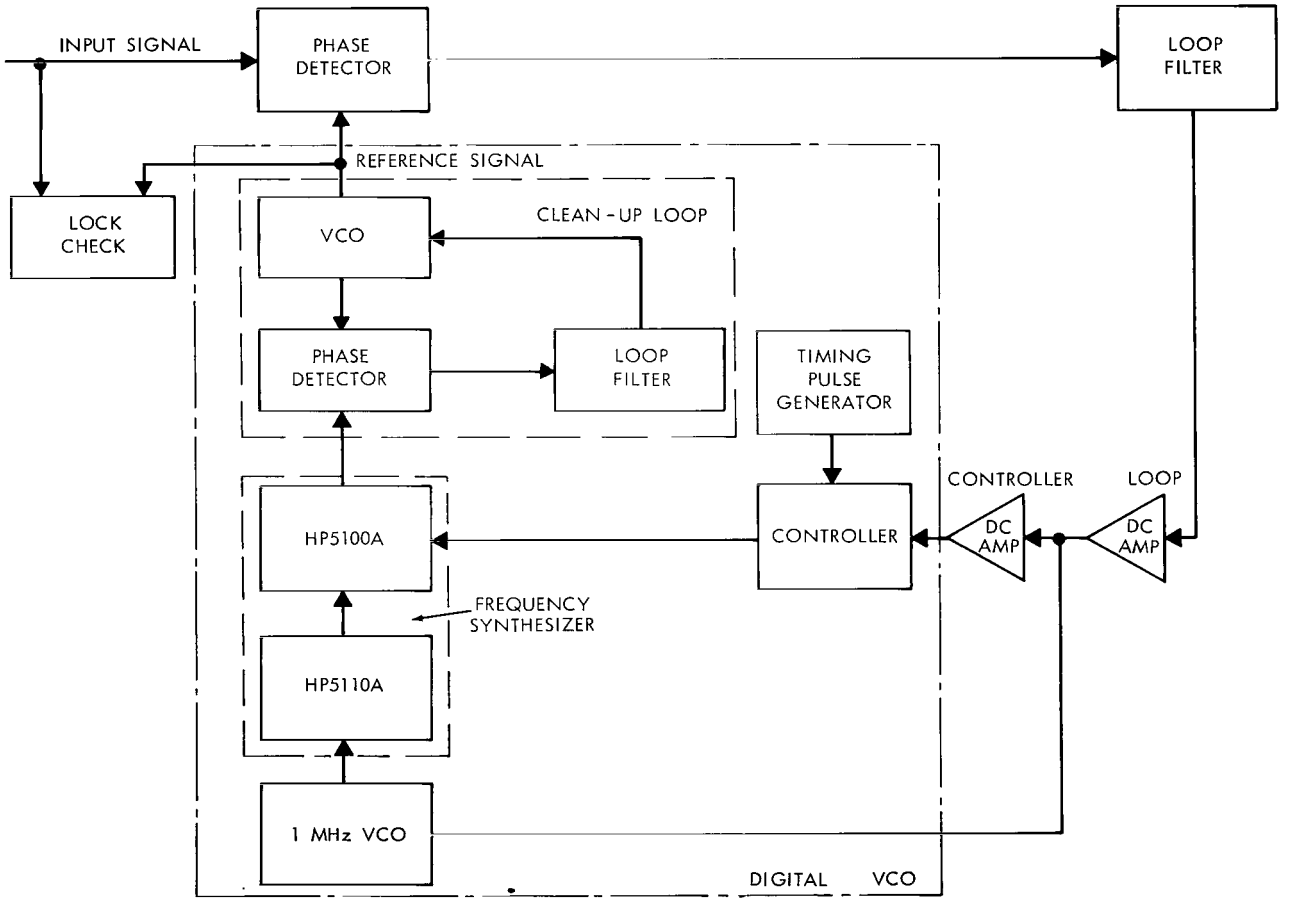

Figure 9—Block diagram of modified digital VCO phase lock loop.

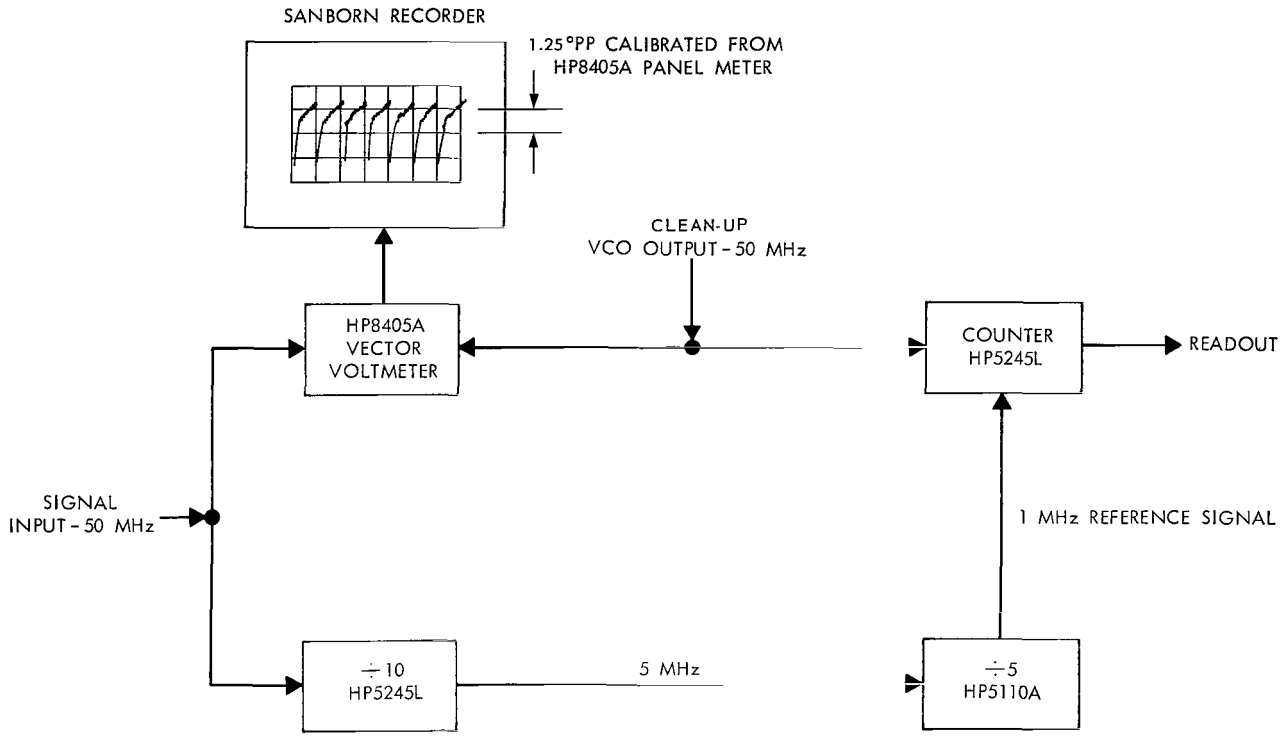

Figure 10—Block diagram of lock-check circuit.

detector. For 10 Hz frequency changes in the synthesizer, peak-to-peak phase errors of approximately 3 degrees were observed (Figure 10). This compares favorably with the results shown in Figure 6.

During this development effort it was assumed that for loop operation it would be necessary to align the synthesizer reference signals in phase and constrain the controller unit to switch the synthesizer in frequency only at an instant when new and old frequencies were in phase (see Appendix A, also Reference 6). To this end, a modification of the HP 5110A driver was made for reference frequency alignment, and the controller was designed to function with a 100 kHz signal synthesized from the aligned reference signals.

Preliminary tests of the loop revealed that reference frequency alignment was unnecessary, because the synthesizer output waveform distortion due to misalignment did not affect loop operation. For the remainder of the experiment, no effort was made to align the reference frequencies or to modify the controller to operate without a 100 kHz signal.

CONCLUSIONS

It has been demonstrated that a coherent frequency synthesizer can be operated as a digital voltage-controlled oscillator in phase lock-loop applications. This gives the advantage of wide frequency-pulling range without sacrificing the frequency stability of the voltage-controlled oscillator. This technique is expected to find wide application in future systems where large doppler shifts are encountered, such as laser communications systems and the Galactic Jupiter Probe.

ACKNOWLEDGMENTS

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Greenbelt, Maryland, October 16, 1967
150-22-14-03-51

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Appendix A

Theory of Operation of Frequency Synthesizer

Figure A1 is a simplified block diagram of the Hewlett-Packard 5100A/5110A Frequency Synthesizer (Reference 7). All frequencies shown are generated from an internal 1-MHz standard oscillator in the HP 5110A Driver Unit or from an external 1 MHz or 5 MHz standard. The driver unit generates a spectrum of frequencies and then appropriately selects 22 fixed frequencies to drive the HP 5100A synthesizer unit. The HP 5100A synthesizer unit contains harmonic generators, dividers, filters, mixers, and amplifiers that arithmetically manipulate the frequencies generated in the driver unit so as to finally produce the desired synthesizer output frequency.

Figure A1 shows two of seven identical mixer-divider units each of which corresponds to a digit of selected output. The mixer divider-unit at the extreme right of the figure produces the least significant digit of the selected frequency. The 24 MHz signal is mixed with 3 MHz to produce 27 MHz, which is then mixed with a selected frequency between 3.0 and 3.9 MHz, a range divided into 100 kHz increments. The selection of this frequency determines the least significant digit of the synthesizer output frequency. The output of the second mixer is therefore a frequency between 30.0 and 30.9 MHz. This frequency is then divided so as to produce a signal between 3.00 and 3.09 MHz. The synthesis process then repeats itself when this frequency is mixed with 24 MHz in the first mixer of the second mixer-divider unit shown. The mixer output frequency of 27.00 to 27.09 MHz is then mixed with a selected frequency within the 3.0 to 3.9 MHz range to give a frequency within the range of 30.00 to 30.99. The signal is divided to give 3.000 to 3.099 MHz. This process repeats itself five more times to obtain a frequency within the range of 3.00000000 to 3.09999999 MHz. Additional mixing produces a signal (0 to 50 MHz) selectable from among 5 billion fixed frequencies all spaced 0.01 Hz apart.

Local selection of the synthesizer output frequency is made at the front panel, by pushbuttons, or remotely, by applying dc voltages to appropriate connector pins at the rear of the HP 5100A synthesizer unit. Either method provides a switching voltage for a diode matrix that selects the appropriate reference frequency (3.0 to 3.9 MHz) to be applied to the mixer-divider unit to produce the digit desired.

The reference signals (3.0 to 3.9 MHz), from which all synthesizer frequencies are derived, are produced in the HP 5110A driver by frequency-multiplication of the 1 MHz standard and by filtering and frequency-dividing a selected harmonic. Frequency division produces randomly phased reference signals. In order to produce a continuous variation of the synthesizer output frequency without distortion, it is necessary to make a numerically ordered selection of phase-coherent reference signals. To achieve this, it is necessary to align the reference signals so that

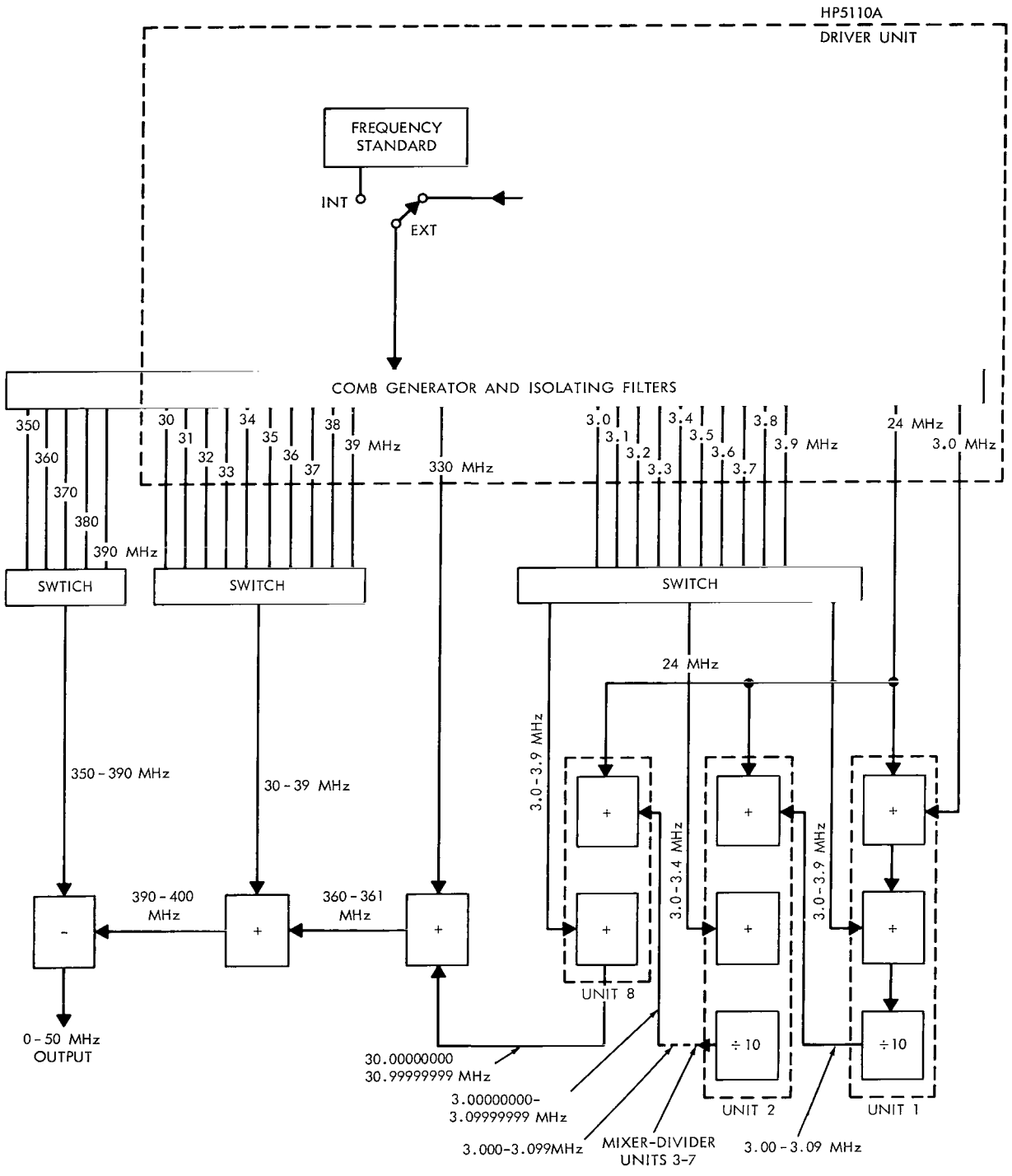

Figure A-1—Simplified block diagram of model HP 5100/5110A frequency synthesizer.

a reference signal is selected at the instant when it and the preceding reference signals are in phase. Since the reference signals are 100 kHz apart in frequency, they would be phase-coherent every 10 microseconds.

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